Electronic Version
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Claims

[c1] 1. A method for fabricating a shallow trench isolation (STI) structure that defines an active area, comprising:
forming a patterned mask layer on a substrate;
forming a doped region in a predetermined depth in the substrate exposed by the mask layer;
forming a shallow trench down to the doped region in the substrate; and
filing an insulating material into the shallow trench.

[c2] 2. The method of claim 1, wherein the step of forming the doped region comprises performing an ion implantation using the mask layer as a mask.

[c3] 3. The method of claim 1, wherein a conductivity type of the doped region is different from a conductivity type of an active device subsequently formed on the active area.

[c4] 4. The method of claim 1, wherein a conductivity type of the doped region is P-type or N-type.

[c5] 5. The method of claim 1, wherein the step of forming the shallow trench comprises performing an etching process to etch the substrate using the mask layer as a mask.

[c6] 6. The method of claim 5, wherein the doped region serves as a detection end point of the etching process.

[c7] 7. The method of claim 1, wherein a thickness of the patterned mask layer exceeds 600Å.

[c8] 8. A shallow trench isolation (STI) structure that defines an active area, comprising:
a shallow trench isolation layer disposed in a shallow trench in a substrate; and
a doped region as a channel stop layer disposed directly under the bottom of the shallow trench isolation layer, wherein
the doped region does not extend to a sidewall of the shallow trench.

[c9] 9. The shallow trench isolation structure of claim 8, wherein a conductivity type of the dopant is different from a conductivity type of an active device disposed on the active area.

[c10] 10. The shallow trench isolation structure of claim 8, wherein the doped region is a P-doped region or an N-doped region.

[c11] 11. A method for fabricating a dynamic random access memory (DRAM) cell, comprising:

forming a trench capacitor in a substrate;
forming a buried strap in the substrate connecting with an upper portion of the trench capacitor;
forming a patterned mask layer on the substrate;
performing an ion implantation to form a doped region of a first conductivity type in a predetermined depth within the substrate exposed by the mask layer;
performing an etching process to etch the substrate down to the doped region to form a shallow trench;
filling an isolating material into the shallow trench;
removing the mask layer;
forming a first doped layer of the first conductivity type in the substrate, wherein the first doped layer is formed at a depth lower than that of the doped region; and
forming an active device on the substrate, the active device being coupled to the trench capacitor via the buried strap.

[c12] 12. The method of claim 11, further comprising forming a second doped layer of a second conductivity type in the substrate electrically connected with a lower electrode of the trench capacitor, the second doped layer being formed at a depth between the doped region and the first doped layer.

[c13] 13. The method of claim 11, wherein the doped region of the first conductivity type serves a detection end point

of the etching process.

[c14] 14. The method of claim 11, wherein the first conductivity type is different from a conductivity type of the active device.

[c15] 15. The method of claim 14, wherein the first conductivity type is P-type.

[c16] 16. The method of claim 11, wherein a thickness of the mask layer is larger than 600Å.

[c17] 17. The method of claim 11, further comprising forming a screen oxide layer on a surface of the substrate after the mask layer is removed.

[c18] 18. A dynamic random access memory (DRAM) cell, comprising:
a trench capacitor in a substrate, including a lower electrode, an inter-electrode dielectric layer and an upper electrode;
a shallow trench isolation layer in the substrate, having a portion encroaching upon the trench capacitor;
a doped region of a first conductivity type in the substrate directly under a bottom of the shallow trench isolation layer;
a first doped layer of the first conductivity type in the substrate lower than the doped region; and

an active device on the substrate coupled to the trench capacitor.

[c19] 19. The DRAM cell of claim 18, wherein the first conductivity type is different from a conductivity type of the active device.

[c20] 20. The DRAM of claim 18, further comprising a second doped layer of a second conductivity type in the substrate electrically connected with the lower electrode of the trench capacitor.

[c21] 21. The DRAM of claim 20, wherein the first doped layer is disposed at a depth between the doped region and the second doped layer.

[c22] 22. The DRAM of claim 18, further comprising a buried strap in the substrate connected with an upper portion of the upper electrode of the trench capacitor, the buried strap coupling the trench capacitor to the active device.